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Low power methodology manual for system-on-chip design pdf

这本ARM和Synopsys合作的《Low Power Methodology Manual》算是Low Power领域的Bible了。既然Synopsys参与了，那里面自然少不了UPF。从作者的背景来看，这本书是偏重实战的，事实的确如此。如果想偏重理论的话，建议看Jan Rabaey的《Low Power Design Essentials》，这本书以后再评。这本《Low Power Methodology Manual》的受众可以涵盖IC架构师、数字前端设计、后端设计、Custom Design等等。虽然说低功耗技术最有用的还是从算法、架构（包括软件）等high level的方面去考虑更有效，但考虑到每款芯片的服务领域并不相同，抽出生性的难度较大，而从low level一点的电路设计来考虑，就有很多共性了，这也是这本书的着重点：low power的电路的设计与物理级实现。前面我们提过，这本书偏重实战，但也是普通SOC芯片flow里的实战。之所以说“普通”，还有一些不普通的低功耗设计技术，比如大名鼎鼎的比特币挖矿芯片，它就不适合用普通的flow去做，否则power上必定是没有什么竞争力的。这本书的重点就是power gating、level shifter和retention这些和power gating及多电压域相关的知识。其实这是其中一个维度，还有一个维度是IR drop、in rush current等问题的解决。学习这本书的时候我们可以把这两个维度结合起来，相信会加深理解。其实我们提到普通低功耗手段，最重要的是clock gating，power gating和voltage scaling，clock gating解决动态功耗，power gating解决静态功耗，voltage scaling则动态静态一起解决。Frequency scaling自然有用，可以降低动态功耗，但这需要结合Performance去考虑，和显式clock gating一样（除了显式clock gating，还有EDA自动综合成的clock gating），不单纯是个电路问题了，可以认为是system architect需要考虑的。至于multi-threshold，一般是标准单元库和EDA要去考虑的事情，designer参与度不高，当然这也是低功耗非常重要的一个手段。要是还想知道知道其他花样，可以参考Jan Rabaey的书，但需要指出的是，里面很多手段在实际中并不常用，有些是随着工艺提升效果不佳的。这本书的语言比较艰涩，通俗点说就是“文绉绉”。我不知道这本书是否有中译版，对于有英文原版的，我强烈建议看英文原版。作为2008年就出版的书，里面还用ARM926EJ-S处理器作为例子，现在来ARM9算是老古董了。但UPF在当时还是属于新生事物，里面所说的技术在今天看则非常主流也不过时。随着EDA的不断改良，它能自动帮我们做的事情越来越多，从这个角度看，低功耗技术的实现实际是EDA和designer的协作过程。综合来看，我给《Low Poweer Methodology Manual》的评级是强烈推荐。 40k Accesses 2 Citations 3 Altmetric Page 2The design of complex chips has undergone a series of revolutions during the last twenty years. In the 1980s there was the introduction of language-based design and synthesis. In the 1990s, there was the adoption of design reuse and IP as a mainstream design practice. In the last few years, design for low power has started to change again how designers approach complex SoC designs.Each of these revolutions has been a response to the challenges posed by evolving semiconductor technology. The exponential increase in chip density drove the adoption of language-based design and synthesis, providing a dramatic increase in designer productivity. This approach held Moore's law at bay for a decade or so, but in the era of million gate designs, engineers discovered that there was a limit to how much new RTL could be written for a new chip project. The result was that IP and design reuse became accepted as the only practical way to design large chips with relatively small design teams. Today every SoC design employs substantial IP in order to take advantage of the ever increasing density offered by sub-micron technology. The "Low Power Methodology Manual" (LPMM) is a comprehensive and practical guide to managing power in system-on-chip designs, critical to designers using 90-nanometer and below technology. The authors, all low power experts, are led by Michael Keating, Synopsys Fellow and principal author of the widely adopted Reuse Methodology Manual for System-on-Chip Design, and David Flynn, ARM R&D Fellow and original architect behind ARM's synthesizable CPU family and the AMBA® on-chip interconnect standard. Combining extensive commercial experience, deep scientific understanding, silicon technology case studies, and a pragmatic approach, the authors describe design techniques which address both dynamic and static (leakage) power, including methods for power gating and dynamic voltage and frequency scaling. For each topic, the authors describe the design challenge, provide a technology foundation, and then make specific recommendations as well as a caution against design pitfalls. This book is a must-read for anyone designing, or getting ready to design, SoCs for low power applications. 查看: 73957|回复: 436 [复制链接] x 本帖最后由 eewater 于 2010-5-7 13:00 编辑 (Synopsys和arm公司联合推出) Editorial ReviewsProduct Description“Tools alone aren't enough to reduce dynamic and leakage power in complex chip designs - a well-planned methodology is needed. Following in the footsteps of the successful Reuse Methodology Manual (RMM), authors from ARM and Synopsys have written this Low Power Methodology Manual (LPMM) to describe [such] [a] low-power methodology with a practical, step-by-step approach.” Richard Goering, Software Editor, EE Times “Excellent compendium of low-power techniques and guidelines with balanced content spanning theory and practical implementation. The LPMM is a very welcome addition to the field of low power SoC implementation that has for many years operated in a largely ad-hoc fashion.” Sujeeth Joseph, Chief Architect - Semiconductor and Systems Solutions Unit, Wipro Technologies “The LPMM enables broader adoption of aggressive power management techniques based on extensive experience and silicon example with real data that every SOC designer can use to meet the difficulties faced in managing the power issues in deep submicron designs.” Anil Mankar, Sr VP Worldwide Core Engineering and Chief Development Officer, Conexant Systems Inc. “Managing power, at 90nm and below, introduces significant challenges to design flow. The LPMM is a timely and immediately useful book that shows how combination of tools, IP and methodology can be used together to address power management.” Nick Salter, Head of Chip Integration, CSR plc. --This text refers to the Hardcover edition. About the AuthorABOUT THE AUTHORS: Michael Keating is a Synopsys Fellow in the company's Advanced Technology Group, focusing on IP development methodology, hardware and software design quality and low power design. David Flynn is an ARM R&D Fellow and has been with the company since 1991, specializing in low power System-on-Chip IP deployment and methodology. Robert Aitken is an ARM R&D Fellow. His areas of responsibility include memory architecture, design for testability and design for manufacturability. Alan Gibbons is a Principal Engineer at Synopsys, with a focus on development of advanced methodology and technology for ARM processor-based system design. Kajian Shi is a Principal Consultant in the Professional Services Group of Synopsys, specializing in low power design methodology and implementation. Low Power Methodology Manual For System-on-Chip Design 读书笔记 登录/注册后可看大图 Low Power Methodology Manual For System-On-Chip Design.pdf 3.91 MB, 下载次数: 6533, 下载积分: 资产 -2 信元, 下载支出 2 信元 收藏14 分享 支持4 反对0 相关帖子